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Application of Zero Average Dynamics and Fixed Point Induction Control Techniques to Control the Speed of a DC Motor with a Buck Converter

Fredy E. Hoyos^{1,*}, John E. Candelo-Becerra²  and Carlos I. Hoyos Velasco³

¹ Faculty of Science, School of Physics, Universidad Nacional de Colombia, Sede Medellín, Carrera 65 No. 59A, 110, Medellín 050034, Colombia

² Faculty of Mines, Department of Electrical Energy and Automation, Universidad Nacional de Colombia, Sede Medellín, Carrera 80 No. 65-223, Robledo, Medellín 050041, Colombia; jecandelob@unal.edu.co

³ Istituto Motori IM, Italian National Research Council, Via Guglielmo Marconi, 4, 80125 Napoli, Italy; c.i.hoyosvelasco@gmail.com

* Correspondence: fehoyosve@unal.edu.co; Tel.: +57-4-4309000

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Abstract: Several technological applications require well-designed control systems to induce a desired speed in direct current (DC) motors. Some controllers present saturation in the duty cycle, which generates variable switching frequency and subharmonics. The zero average dynamics and fixed point induction control (ZAD-FPIC) techniques have been shown to reduce these problems; however, little research has been done for DC motors, considering fixed switching frequency, quantization effects, and delays. Therefore, this paper presents the speed control of a DC motor by using a buck converter controlled with the ZAD-FPIC techniques. A fourth-order, non-linear mathematical model is used to describe the system dynamics, which combines electrical and electromechanical physical models. The dynamic response and non-linear system dynamics are studied for different scenarios where the control parameters are changed. Results show that the speed of the motor is successfully controlled when using ZAD-FPIC, with a non-saturated duty cycle presenting fixed switching frequency. Simulation and experimental tests show that the controlled system presents a good performance for different quantization levels, which makes it robust to the resolution for the measurement and type of sensor.

Keywords: DC–DC buck converter; DC motor; bifurcations; control parameter; sliding control; speed control

1. Introduction

Direct current (DC) motors are very important electromechanical devices in mechatronic systems, which play a fundamental role in the execution of high precision tasks [1]. With the recent advances in permanent magnet materials, as well as their characteristics, such as being lighter, low cost, and low speed, industrial and residential users have increased their use [2,3]. However, non-linear phenomena, such as bifurcations and chaos, have been observed in many types of motor actuators; hence, the behavior of the controller with different resolutions in the measured signals must be identified [4–6].

In [7,8], a sliding-mode control is developed to drive an induction motor without sensors; for this, direct torque control and space vector pulse width modulation (SVPWM) are used, where a sliding mode observer using a dual reference frame motor model is introduced and tested. In [9], an adaptive sliding mode controller for the induction motor speed without mechanical sensors is presented. Also in [10], a robust and adaptable sliding controller is formulated for single-input and single-output

(SISO) non-linear systems, with application in a linear induction motor. Some drawbacks of the sliding mode control are [10–12] that the control gain is large when the limits of the defined parameters are large; the control input may show chattering, which may cause high frequency; and chattering in the input can cause high energy consumption and wear of mechanical components [13,14]. The quasi-sliding mode control emerged as an alternative solution to the inconveniences of the sliding mode control, while retaining the inherent advantages of its operation. In fact, chattering and high frequency switching of the control signal are avoided.

On the other hand, for experimental tests, the digital signal processor (DSP) offers the following features: greater versatility and flexibility compared to analog designs [15], ease in the implementation of non-linear controllers and advanced control techniques, low power consumption and reduction of external passive components, applications with high switching frequency controllers, and others [16–19].

The quantization effects of the signals in the experimental test (state variables, the duty cycle, etc.) can cause unwanted oscillations, limit cycles, periodic bands, and chaotic behavior [20–23]. Additionally, according to [16], where the authors study the dynamic response of controlled systems in digital devices, time delays at controller outputs can cause instability [24]. Likewise, in [20] the limit cycles presented in electronic power converters controlled with digital pulse width modulation (DPWM) are set out. To avoid such oscillations, some conditions are imposed on the control law and quantization limits [20]. The fixed point induction control (FPIC) technique allows the stabilization of unstable orbits, as presented in [25], and also allows the estimation of unknown and variable parameters in power converters [26,27]. The minimum requirements for the digital controller parameters are determined in [17], which include the sampling time and the resolution in the measured variables.

In [28], a dynamic sliding surface is used to apply the zero averaging error dynamics control technique (ZAD) as a quasi-sliding mode alternative. ZAD control is also used for the implementation of a buck inverter in an field-programmable gate array (FPGA), verifying that the ZAD technique with side pulse meets the requirement of fixed switching frequency [29,30]. In [31], the numerical and experimental results obtained by applying digital control implemented in a DSP are presented, using the ZAD-FPIC technique in DC–DC and DC–alternating current (AC) converters. From this study, the bifurcation diagrams calculated numerically in the design stage agree quantitatively with those obtained in the experimental test. In works such as [25–27,32], the integration of ZAD and FPIC techniques show good results in variable regulation, using buck converters with resistive and motor loads. The ZAD-FPIC technique has been applied in second-order systems, however there are no bifurcation analyses for the FPIC technique.

All these applications show that the ZAD-FPIC technique integrates well with the buck converter, achieving good regulation and tracking of signals at the output when the load is resistive. In addition, with this technique the chattering problem is avoided and the fixed switching frequency is obtained, which is appropriate for control of motors and electromechanical applications. However, in the case of non-resistive loads, e.g. DC motors, few studies have been carried out [26], creating the need for a detailed study that considers the parameter adjustment of the control law, and the effects of numerical quantization, delays, bifurcations, and chaos behavior. As previously reported in the literature, controllers cause saturation in the duty cycle, creating variable switching frequency and sub-harmonics. This problem has been solved by the applying ZAD-FPIC technique for resistive loads; however, electromechanical systems that consider the quantization effects and delays (to obtain a fixed switching frequency in the switches) have not been used, which are more interesting for industrial applications.

Therefore, this paper shows the application of the ZAD-FPIC technique to control the speed of a DC motor using a buck converter as an electric actuator. Additionally, quantization effects are included in the system variables and bifurcation diagrams are obtained to show the behavior when the control parameters are changed. Some of the advantages of using ZAD-FPIC techniques are that the controller presents a fixed switching frequency, low steady-state error, and robustness for the time delays in the system. In [6], some advantages of using ZAD-FPIC techniques to control the buck converter are shown

after comparing this controller to the sliding mode control (SMC) and proportional–integral–derivative (PID) techniques. However, this technique is not robust to changes in the system parameters, and the real-time processing requires a high sampling rate and synchronization of signal sensing with a centered pulse width modulation (CPWM) output [33]. Additionally, the design of the controller becomes very complicated when it is used to control higher order systems (more than 6 linear differential equations).

Hence, to present the development of this control application, the paper is divided into four more sections. Section 2 presents the materials and methods used in the research, as well as the mathematical modelling required to design the controller using the ZAD-FPIC technique and to perform the closed loop control simulations. Section 3 includes the results and analysis of the different simulation and experimental tests performed with the proposed changes in the control parameters. Finally, Section 4 ends the paper presenting the conclusions.

2. Materials and Methods

Figure 1 shows the block diagram of the studied system, which is divided into software and hardware. In particular, from system schematics it is shown that the control implementation includes the hardware part with physical and electronic components, while the software part uses a DSP to acquire/process signals and to implement the control technique.

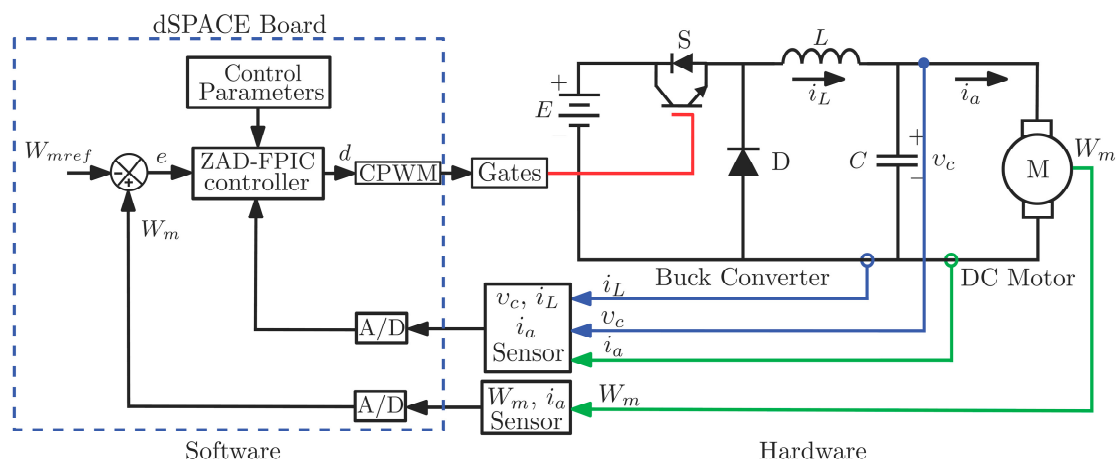


Figure 1. Diagram of the buck converter with zero average dynamics and fixed point induction control (ZAD-FPIC) techniques to control the speed of a direct current (DC) motor. CPWM, centered pulse width modulation.

The hardware consists of a permanent magnet DC motor that has the following characteristics: nominal power of 250 W, supply voltage of 42 V, nominal current of 6 A, and maximum speed of 4000 RPM. To measure the speed of the motor (W_m), an encoder with a rating of 1000 pulses per revolution was used. For sensing of the state variables, namely the capacitor voltage (v_c), inductor current (i_L), and a motor armature current (i_a), some precision resistors were used. The digital part is developed using the DS1104 board in dSPACE [34,35], in which the ZAD-FPIC technique is implemented. The output of the centered pulse width modulation (CPWM) is calculated in real time by the DS1104.

The state variables v_c , i_L , and i_a arrive at the controller through the 12-bit analog–digital (ADC) inputs. The controlled variable W_m is measured by an encoder that has 28 bits. All these variables are acquired at a sampling rate of 6 kHz. The control block admits the constant parameters defined for the DC electric motor, buck converter, and the ZAD-FPIC technique. The last required parameters are related to the time constants and the dynamics of the error that are imposed on the control system, for example K_{S1} , K_{S2} , and K_{S3} as described in following sections. During each sampling period, the microprocessor in the DS1104 board computes the duty cycle, namely d , with 10-bit resolution, along with its equivalent in the centered pulse width modulation (CPWM) signal for control gate

of the metal oxide semiconductor field effect transistor (MOSFET). Table 1 presents the values of the parameters of the power converter, the motor, and the controller. By using the method of [36], system parameters have been measured experimentally.

Table 1. Parameters of the controller and the circuit.

Parameter	Description	Value
r_s	Total resistance at the source	0.84 Ω
E	Power supply voltage	40.086 V
V_{fd}	Forward voltage	1.1 V
L	Inductance	2.473 mH
r_L	Total resistance in the inductor	1.695 Ω
C	Capacitance	46.27 μF
R_a	Armature resistance	2.7289 Ω
L_a	Armature inductance	1.17 mH
B	Viscosity friction coefficient	0.000138 (N·m/(rad/s))
J_{eq}	Inertia moment	0.000115 (kg·m ²)
k_t	Motor torque constant	0.0663 (N·m/A)
k_e	Motor voltage constant	0.0663 (V/rad/s)
T_{fric}	Friction constant	0.0284 (N·m)
T_L	Load torque	Variable (N·m)
W_{mref}	Speed reference	Variable (rad/s)
W_m	Speed of the DC motor	Variable (rad/s)
N	Control parameter of the FPIC	1
F_c	Switching frequency	6 kHz
F_s	Sampling frequency	6 kHz
$1T_p$	Delay period	166.6 μs
K_{S1}	Control parameter	2
K_{S2}	Control parameter	2
K_{S3}	Control parameter	Variable

2.1. Model of the Buck Converter with a DC Motor

The DC motor and mechanical load are modeled by Equations (1) and (2), which correspond to the electromechanical part of the system, described by a second order mathematical model, where the state variables are the speed of the DC motor (W_m) in rad/s and the armature current (i_a) in amps.

$$\dot{W}_m(t) = \frac{-BW_m(t)}{J_{eq}} + \frac{k_t i_a(t)}{J_{eq}} + \frac{-T_{fric}}{J_{eq}} + \frac{-T_L}{J_{eq}} \quad (1)$$

$$i_a(t) = \frac{-k_e}{L_a} W_m(t) + \frac{-R_a}{L_a} i_a(t) + \frac{V_a}{L_a} \quad (2)$$

The term k_e is the voltage constant (V/rad/s) of the motor, L_a is the armature inductance (mH), R_a is the armature resistance (Ω), V_a is the voltage applied to the motor (V) and is equal to v_c , B is the viscous friction coefficient (N·m/(rad/s)), J_{eq} is the moment of inertia (kg·m²), k_t is the motor torque constant (N·m/A), T_{fric} is the friction torque (N·m), and T_L is the load torque (N·m).

Figure 2 shows that the complementary part of the electrical subsystem corresponds to the circuit of the buck converter. The mechanical subsystem corresponds to the rotating mechanical part of the motor and the mechanical load connected to it. Here, the way in which the output of the buck converter feeds the DC motor with a regulated voltage is illustrated. The presented configuration allows the speed of the motor to be controlled in a closed loop, manipulating the state of the switch (S = ON and S = OFF); that is, the control gate of MOSFET transistor.

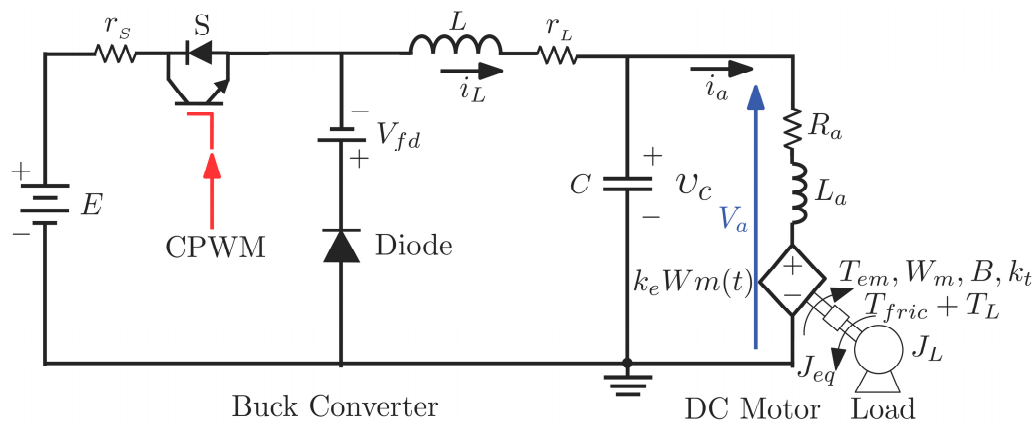


Figure 2. Electromechanical system for speed control of a DC motor powered by a buck converter.

The state variables of the buck converter with the motor depends on the state of the switch (S). Thus, if the switch is closed (S = ON) and the diode is not conducting (inactive), the system is represented as described in Equation (3).

$$\begin{bmatrix} \dot{W}_m \\ \dot{i}_a \\ \dot{v}_c \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} \frac{-B}{J_{eq}} & \frac{k_t}{J_{eq}} & 0 & 0 \\ \frac{-k_e}{L_a} & \frac{-R_a}{L_a} & \frac{1}{L_a} & 0 \\ 0 & \frac{-1}{C} & 0 & \frac{1}{C} \\ 0 & 0 & \frac{-1}{L} & \frac{-(r_L+r_s)}{L} \end{bmatrix} \begin{bmatrix} W_m \\ i_a \\ v_c \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{-(T_{fric}+T_L)}{J_{eq}} \\ 0 \\ 0 \\ \frac{E}{L} \end{bmatrix} \quad (3)$$

In a compact form, it can be represented as shown in Equation (4), where $x_1 = W_m$, $x_2 = i_a$, $x_3 = v_c$, and $x_4 = i_L$.

$$\dot{x} = A_1x + B_1 \quad (4)$$

When the switch is open (S = OFF) and the diode is conducting, the model is described as presented in Equation (5).

$$\begin{bmatrix} \dot{W}_m \\ \dot{i}_a \\ \dot{v}_c \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} \frac{-B}{J_{eq}} & \frac{k_t}{J_{eq}} & 0 & 0 \\ \frac{-k_e}{L_a} & \frac{-R_a}{L_a} & \frac{1}{L_a} & 0 \\ 0 & \frac{-1}{C} & 0 & \frac{1}{C} \\ 0 & 0 & \frac{-1}{L} & \frac{-r_L}{L} \end{bmatrix} \begin{bmatrix} W_m \\ i_a \\ v_c \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{-(T_{fric}+T_L)}{J_{eq}} \\ 0 \\ 0 \\ \frac{-V_{fd}}{L} \end{bmatrix} \quad (5)$$

This last equation can be written in compact form as shown in Equation (6).

$$\dot{x} = A_2x + B_2 \quad (6)$$

The system described above by Equations (3) and (5) is of the fourth order. Parameters C and L are the capacitance and the inductance of the power converter, respectively. The total resistance at the source (r_s) is equal to the sum of the internal resistance of the source (r_{ss}) and the resistance of the MOSFET (r_M), as presented in Equation (7). The total resistance in the inductor (r_L) is equal to the sum of the resistance in the coil (r_{LL}) and the resistance used to measure the current in the inductor (r_{Med}), as presented in Equation (8).

$$r_s = r_{ss} + r_M \quad (7)$$

$$r_L = r_{LL} + r_{Med} \quad (8)$$

The term V_{fd} is the forward voltage and E is the power supply voltage, corresponding to the value that feeds the buck converter and the DC motor when the state of switch S is active. Note when S is inactive $-V_{fd}$ is fed to buck converter. Considering that the CPWM signal is configured with a

pulse in the center and the buck converter works in continuous conduction mode, the dynamics of the system over a full period are described by the Equation (9).

$$\dot{x} = \begin{cases} A_1x + B_1 & si & kT \leq t \leq kT + dT/2 \\ A_2x + B_2 & si & kT + dT/2 < t < kT + T - dT/2 \\ A_1x + B_1 & si & kT + T - dT/2 < t < kT + T \end{cases} \quad (9)$$

2.2. Speed Control of a DC Motor

As a speed control is applied to the DC motor W_m , the reference speed W_{mref} must be followed in the rotary load. Thus, in the sampling period kT , the tracking error is defined in Equation (10):

$$e(kT) = W_m(kT) - W_{mref}(kT) \quad (10)$$

Furthermore, by considering that the system is of fourth order, the sliding surface $s(x)$ [29] describes the third order dynamic behavior of the error ($e(kT)$), given by Equation (11):

$$s(kT) = e(kT) + k_{s1} \frac{de(kT)}{d(kT)} + k_{s2} \frac{d^2e(kT)}{d(kT)^2} + k_{s3} \frac{d^3e(kT)}{d(kT)^3} \quad (11)$$

The coefficients k_{s1} , k_{s2} , and k_{s3} are parameterized as a function of the constant of the inductive-capacitive (LC) filter multiplied by the factors K_{S1} , K_{S2} , and K_{S3} , as shown in Equation (12). The factors K_{S1} , K_{S2} , and K_{S3} are the parameters of the ZAD controller and can be adjusted to impose a desired dynamic in the closed loop system. Note that, such parameters can be considered to construct dimensional bifurcation diagrams.

$$\begin{aligned} k_{s1} &= K_{S1} \sqrt{LC} \\ k_{s2} &= K_{S2} LC \\ k_{s3} &= K_{S3} LC \sqrt{LC} \end{aligned} \quad (12)$$

When the reference signal W_{mref} is constant, Equation (11) can be written as shown in Equation (13), and the derivate is equal to Equation (14):

$$s(kT) = W_m(kT) - W_{mref}(kT) + k_{s1} \frac{dW_m(kT)}{d(kT)} + k_{s2} \frac{d^2W_m(kT)}{d(kT)^2} + k_{s3} \frac{d^3W_m(kT)}{d(kT)^3} \quad (13)$$

$$\dot{s}(kT) = \frac{dW_m(kT)}{d(kT)} + k_{s1} \frac{d^2W_m(kT)}{d(kT)^2} + k_{s2} \frac{d^3W_m(kT)}{d(kT)^3} + k_{s3} \frac{d^4W_m(kT)}{d(kT)^4} \quad (14)$$

The duty cycle can be calculated as expressed in Equation (15):

$$d_k(kT) = \frac{2s(kT) + T\dot{s}_-(kT)}{T(\dot{s}_-(kT) - \dot{s}_+(kT))} \quad (15)$$

where $s(kT)$ is calculated with Equation (11) at the beginning of each switching period for the system given in Equation (3). Thus, $s(kT) = s(kT)|_{S=ON}$; $\dot{s}_+(kT)$ is calculated with Equation (12) for the system given in Equation (3); that is, $\dot{s}_+(kT) = \dot{s}(kT)|_{S=ON}$. Additionally, the parameter $\dot{s}_-(kT)$ is calculated with Equation (14) for the system given by Equation (5); that is, $\dot{s}_-(kT) = \dot{s}(kT)|_{S=OFF}$.

Given the period of delay in the control action, the new duty cycle is calculated, as in Equation (16).

$$d_k(kT) = \frac{2s((k-1)T) + T\dot{s}_-((k-1)T)}{T(\dot{s}_-((k-1)T) - \dot{s}_+((k-1)T))} \quad (16)$$

By considering the ZAD-FPIC technique, the new duty cycle is calculated to ensure that the load and the motor rotate at the desired speed (W_{mref}), leading to the expression for the duty cycle given in Equation (17).

$$d_{ZADFPIC}(kT) = \frac{d_k(kT) + Nd^*}{N + 1} \tag{17}$$

Combining Equations (16) and (17), the following control law of the ZAD-FPIC is obtained, as shown in Equation (18):

$$d_{ZADFPIC}(kT) = \left(\frac{2s((k-1)T) + T\dot{s}_-((k-1)T)}{T(\dot{s}_-((k-1)T) - \dot{s}_+((k-1)T))} + Nd^* \right) (N + 1)^{-1} \tag{18}$$

where d^* is calculated at the beginning of each period, as shown in Equation (19):

$$d^* = d_k(kT)|_{estado\ estable} \tag{19}$$

Finally, a saturation function must be applied to consider the actual physical limits of the duty cycle between 0 and 1, leading to the saturation function described in Equation (20):

$$d = \begin{cases} d_{ZADFPIC}(kT) & \text{if } 0 < d_{ZADFPIC}(kT) < 1 \\ 1 & \text{if } 1 \leq d_{ZADFPIC}(kT) \\ 0 & \text{if } d_{ZADFPIC}(kT) \leq 0 \end{cases} \tag{20}$$

3. Results and Analysis

This section shows the numerical and experimental results for the speed control of a DC motor using a buck converter controlled with the ZAD-FPIC technique. The results are divided into results obtained for the transient and steady states.

3.1. Transient-State Results

The results were obtained according to the quantization effects, defined as: $W_m = 28$ bits, ADC 12 bits (i_a, v_c, i_L), and d 10 bits, with $K_{S1} = 2, K_{S2} = 2, K_{S3} = 30$, and $N = 1$, leading to a delay of one period.

Figure 3a shows the speed of the motor for the simulation test (black), the speed of the motor for the experimental test (blue), and the reference speed (W_{mref}). Initially, it starts from a reference speed ($W_{mref} = 100$ rad/s). Then, at $t = 1$ s the reference signal changes ($W_{mref} = 400$ rad/s) and Figure 3c shows the numerical error (black) and the experimental error (blue) of the DC motor speed signals (W_m). Considering the overshoot (OS), the settling time (ST), and the steady-state error (SSError) as performance indices of the control technique, Figure 3a shows the OS, with a value of 0.57% for the simulation test and a 0% for the experimental test, while the SSError are -0.1645% and 0.4245% for the simulation and experimental results, respectively. Additionally, the experimental results in Figure 3a confirm the predictions obtained by the numerical simulations. Considering the settling time for the controlled variable W_m , the numerical simulation produces a value of $ST = 0.1473$ s, while the experimental value is of $ST = 0.1859$ s, as shown in Table 2.

Table 2. Performance of the closed loop system: overshoot (OS), settling time (ST), and steady-state error (SSError).

Index	Simulation Test	Experimental Test
OS (%)	0.57	0
ST (seg)	0.1473	0.1859
SSError (%)	-0.1645	0.4245

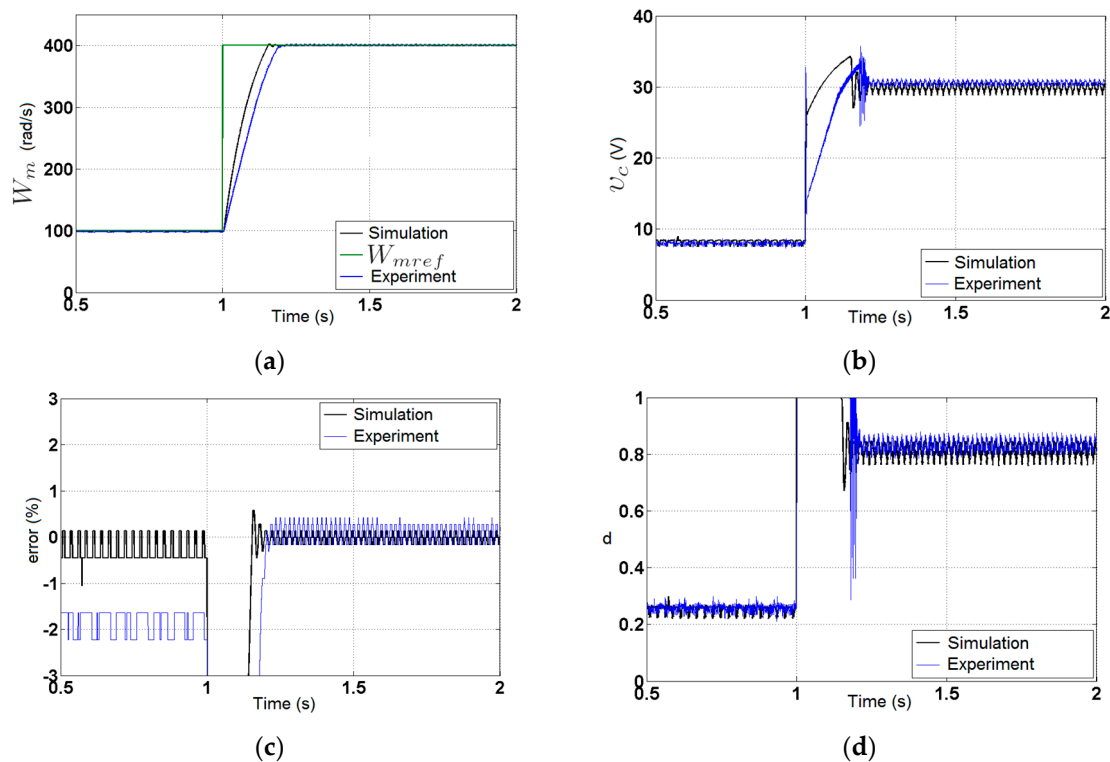


Figure 3. Numerical and experimental behavior when there is a change in the speed reference signal (W_{mref}): (a) motor speed signals (W_m); (b) motor supply voltage ($V_a = v_c$); (c) speed error; and (d) duty cycle.

Figure 3b shows the motor supply voltage ($V_a = v_c$) for the simulation (black) and experimental (blue) tests, with very similar behavior shown for both the steady- and transient-state stability, although with a slight difference in time delay for the transient state. It is important to note that the supply voltage of the DC motor does not exceed 36 volts and that this has a low ripple during the steady state, which is optimal for the proper functioning of the DC motor and for maintaining the speed (W_m) with low steady-state error. Figure 3d confirms that the duty cycle (d) is not saturated during the steady state, which would generate a CPWM signal with fixed switching frequency.

In Figure 3, there are some small differences between the results obtained with the simulation and the experiment, especially in the transient state. The experiment shows a longer setup time and less overshoot, because in the simulation test the parasitic resistor of the capacitor in the buck converter was not considered. Additionally, in the steady state there are also small differences between the simulation and experimental results, because the resistance used to measure the current in the inductor (r_{Med}) increases when the temperature of the shunt resistor r_{Med} increases.

3.2. Steady-State Results

Here, this manuscript presents the results for the steady-state operation of the buck converter with a DC motor that is controlled by the ZAD-FPIC technique are presented. The goal of this analysis is to present the dynamic behavior of the closed loop system when the control parameter K_{S3} changes. An additional purpose is to define a tuning criteria for control parameters, while evaluating the dynamic characteristics of the system stability via bifurcations diagrams. The control parameter K_{S3} defined in Equation (10) was selected as the bifurcation parameter because this parameter is more sensible than the two others control parameters (K_{S1} and K_{S2}).

Figures 4 and 5 show numerical and experimental results of the duty cycle and the motor speed with respect to the control parameter K_{S3} , respectively. Three different quantization levels were considered for the variables as follows. Firstly, W_m with 28 bits; i_a , v_c , and i_L , each with 12 bits; and a

duty cycle of 10 bits. Secondly, W_m with 26 bits; i_a , v_c , and i_L , each with 10 bits; and a duty cycle of 8 bits. Thirdly, W_m with 24 bits; i_a , v_c , and i_L , each with 8 bits; and a duty cycle of 6 bits.

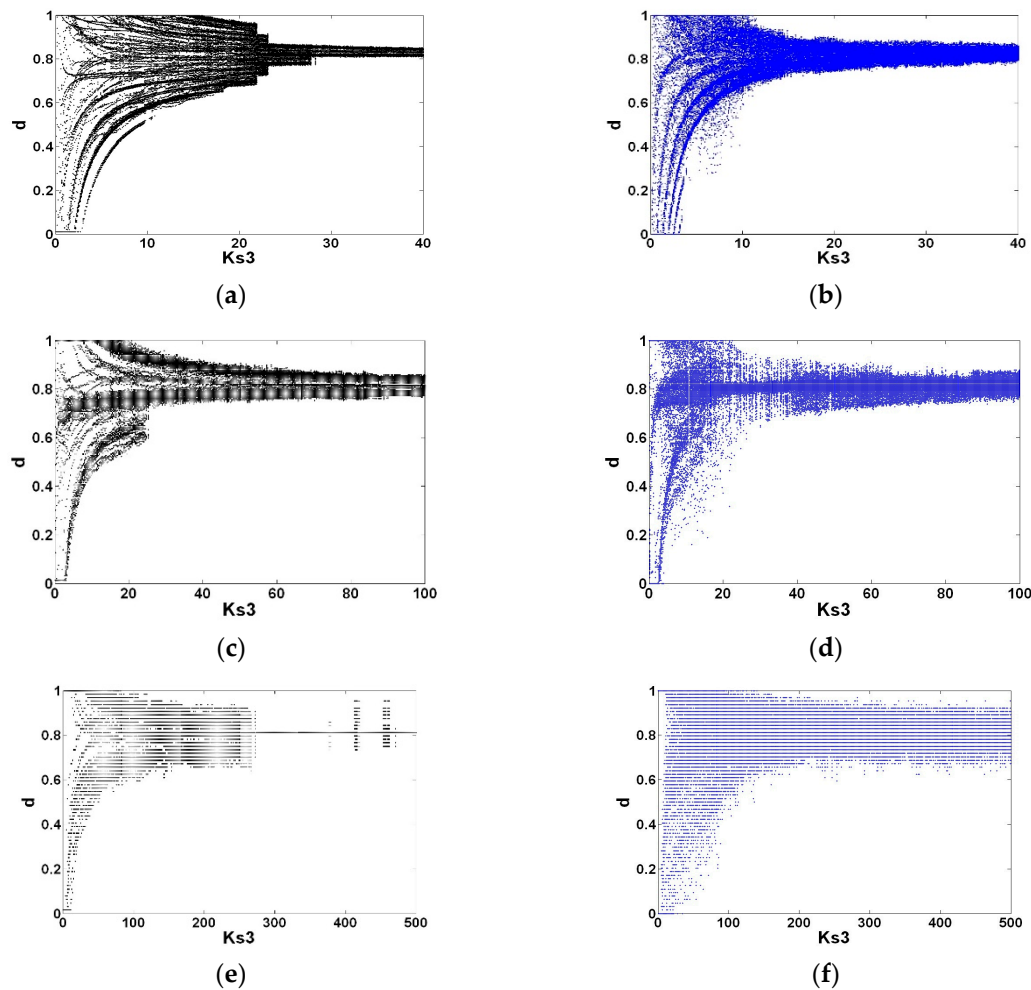


Figure 4. Numerical and experimental bifurcation diagrams for the duty cycle d with respect to the control parameter K_{S3} . These diagrams are plotted considering the following quantization levels: (a) W_m with 28 bits, analog–digital (ADC) inputs with 12 bits, d with 10 bits; (b) W_m with 28 bits, ADC with 12 bits, and d with 10 bits; (c) W_m with 26 bits, ADC with 10 bits, and d with 8 bits; (d) W_m with 26 bits, ADC with 10 bits, and d with 8 bits; (e) W_m with 24 bits, ADC with 8 bits, and d with 6 bits; and (f) W_m with 24 bits, ADC with 8 bits, and d with 6 bits.

In the experimental test, the steady-state error is higher when the resistance r_{Med} increases, for which the bifurcation diagrams presented in Figure 4 show a slight difference between the simulation and experimental results. To improve this difference, it is recommended to perform a better calibration of the parasitic resistance, along with real-time sensing of the resistances r_{Med} , r_L , and r_s . Thus, a greater correlation between the simulation and experimental results can be found.

In general, Figures 4 and 5 show a good correlation between numerical and experimental results. Figure 4a shows that for the highest quantization levels, the stability limit at the numerical test has a value close to $K_{S3} = 22$, while for the experimental test (Figure 4b) this value is $K_{S3} = 12$. For the lowest quantization level, the numerical test (Figure 4e) shows that the stability limit is close to $K_{S3} = 270$, while for the experimental test (Figure 4f) it is $K_{S3} = 170$. Therefore, from these results we can conclude that the experimental test presents a more stable behavior for lower values of K_{S3} , and that as the quantization levels are reduced for both the simulation and experimental tests, the stability is lost and it is necessary to increase the value of K_{S3} to obtain stability in the controlled signal W_m .

Figure 5 shows that there is no clear stability limit, however by means of the duty cycle d it can be measured when the stability is lost. Both numerical and experimental tests showed that the system begins to be more unstable and that the bifurcation point moves to the right because of resolution lost in the measured variables. For all quantization levels, the responses of the controller were good and the regulation was performed to the desired reference point. However, some small differences between the experimental and simulated results were found during the tests for all cases.

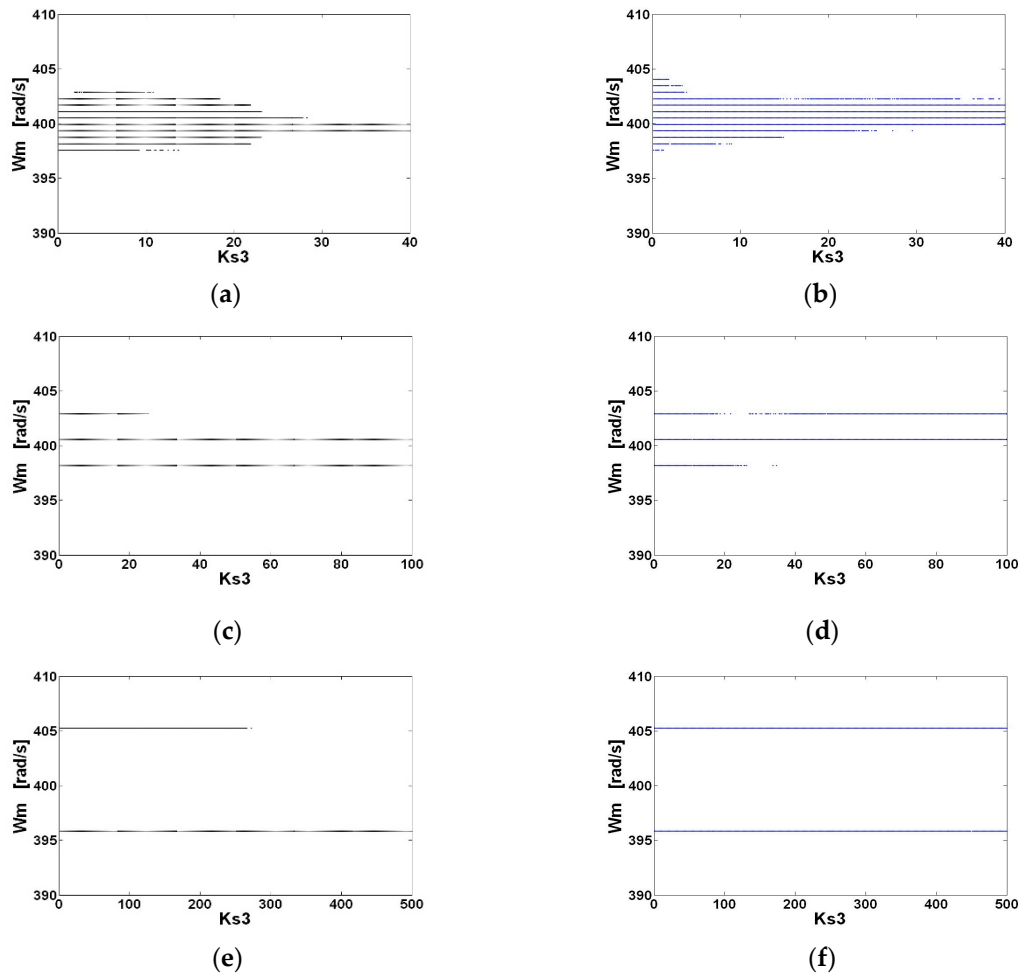


Figure 5. Numerical and experimental bifurcation diagrams for the speed of the motor W_m versus the control parameter K_{S3} . These diagrams are plotted considering the following quantization levels: (a) W_m with 28 bits, ADC with 12 bits, and d with 10 bits; (b) W_m with 28 bits, ADC with 12 bits, and d with 10 bits; (c) W_m with 26 bits, ADC with 10 bits, and d with 8 bits; (d) W_m with 26 bits, ADC with 10 bits, and d with 8 bits; (e) W_m with 24 bits, ADC with 8 bits, and d with 6 bits; and (f) W_m with 24 bits, ADC with 8 bits, and d with 6 bits.

4. Conclusions

This paper presented a speed control for a DC motor performed with the ZAD-FPIC technique. The results showed that the buck converter with the motor controlled by the ZAD-FPIC technique achieved good speed regulation, imposing the desired rotation value by means of the reference signal. Additionally, the bifurcation diagrams showed that the ZAD-FPIC technique allowed the closed-loop control of the speed in an electric motor, using a buck converter as an electric actuator. This can generate a speed regulation error of less than 3% for the entire range of variation of K_{S3} , with $K_{S1} = K_{S2} = 2$, a delay period, and $N = 1$. The numerical and experimental tests showed that even with low quantization levels in the measured variables and in the PWM signal, the buck converter with the motor

controlled by the ZAD-FPIC technique had good speed regulation. Finally, for the higher quantization limits, the system obtained low values for overshoot (OS), settling time (ST), and steady-state error (SSError).

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Abbreviations

ADC	Analog-to-digital converter
AC	Alternating current
CPWM	Centered pulse width modulation
DC	Direct current
DPWM	Digital pulse width modulation
DSP	Digital signal processor
FPGA	Field-programmable gate array
FPIC	Fixed point induction control
LC	Inductive-capacitive
MOSFET	Metal–oxide–semiconductor field-effect transistor
OS	Overshoot
PID	Proportional integral derivative
PWM	Pulse-width modulation
SISO	Single-input and single-output
SMC	Sliding mode control
SSError	Steady-state error
ST	Settling time
SVPWM	Space vector pulse width modulation
ZAD	Zero average dynamics
ZAD-FPIC	Zero average dynamics and fixed point induction control

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